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A Feedback Wideband CMOS LNA Employing Active Inductor-Based Bandwidth Extension Technique

Jaeyoung Choi*, Sanggil Kim*, and Donggu Im**

Abstract

A bandwidth-enhanced ultra-wide band (UWB) CMOS balun-LNA is implemented as a part of a software defined radio (SDR) receiver which supports multi-band and multi-standard. The proposed balun-LNA is composed of a single-to-differential converter, a differential-to-single voltage summer with inductive shunt peaking, a negative feedback network, and a differential output buffer with composite common-drain (CD) and common-source (CS) amplifiers. By feeding the single-ended output of the voltage summer to the input of the LNA through a feedback network, a wideband balun-LNA exploiting negative feedback is implemented. By adopting a source follower-based inductive shunt peaking, the proposed balun-LNA achieves a wider gain bandwidth. Two LNA design examples are presented to demonstrate the usefulness of the proposed approach. The LNA I adopts the CS amplifier with a common gate common source (CGCS) balun load as the S-to-D converter for high gain and low noise figure (NF) and the LNA II uses the differential amplifier with the ac-grounded second input terminal as the S-to-D converter for high second-order input-referred intercept point (IIP2). The 3 dB gain bandwidth of the proposed balun-LNA (LNA I) is above 5 GHz and the NF is below 4 dB from 100 MHz to 5 GHz. An average power gain of 18 dB and an IIP3 of -8 ~ -2 dBm are obtained. In simulation, IIP2 of the LNA II is at least 5 dB higher than that of the LNA I with same power consumption.

Keywords : CMOS, common drain, common source, feedback, inductive shunt peaking, LNA, SDR, UWB

Ⅰ. INTRODUCTION

Most recent and interesting evolutions in the RF receivers are the trends toward software defined radio (SDR) receivers for supporting multi-bands and multi-standards based on a single chip and Saw-less receivers that can eliminate many SAW filters required for the commercial mobile handsets. The receivers satisfying simultaneously the requirements of SDR and Saw-less receivers are called as Saw-less SDR receivers (SSDRR) in this paper. RF front-end circuits for SSDRR should support wide frequency range with sufficiently high gain and low noise figure (NF) for meeting the sensitivity requirement of as many standards as possible. Also, in order to overcome the distortion problem such as desensitization, gain compression, inter-modulation, and cross-modulation without help of SAW filters, the RF front-end circuits should have ultra-high linearity and spur free dynamic range (SFDR).

The LNA design approach for the SSDRR can be divided into two categories: the multiple tuned narrowband LNA and the single wideband LNA. In the case of the multiple tuned narrowband LNAs, their

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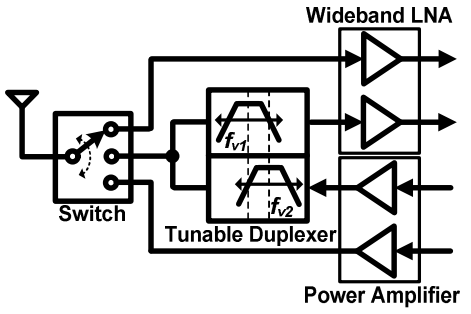


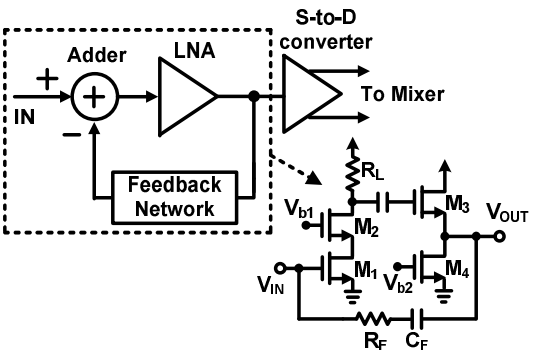
Fig. 1. Front-end Architectures for Saw-less SDR Receiver supporting both FDD and TDD communication standard.

complexity and occupied chip area grow rapidly as the number of covered standards increases. Also, these LNAs should have control circuits to automatically tune the design parameters for achieving stable performances over PVT variations. Therefore, adopting a single wideband LNA is desirable because it can satisfy the requirements of any standard in a wide frequency range with low complexity and cost. However, the SFDR performance of conventional wideband LNAs should be improved in order to receive a weak wanted signal with large undesired-to-desired (U/D) ratios without SAW filters. As shown in Fig. 1, in combination with a tunable RF filter/duplexer having a relaxed stop band attenuation level compared to commercial SAW filters, this LNA with ultra-high SFDR seems to be a straightforward and a cost-effective solution for the SSDRR. The assumption here is that MEMS or SOI CMOS switches with high power capability capable of tunable RF selectivity will be available in a near future.

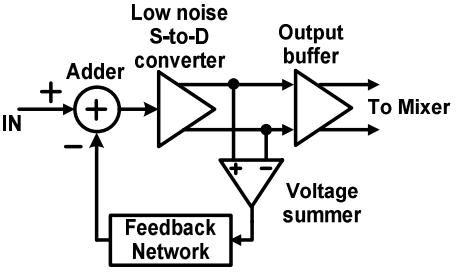
In this paper, an active feedback wideband single-to-differential (S-to-D) LNA using inductive shunt-peaking for the SSDRR is proposed.

Ⅱ. Proposed Balun-LNA (LNA I)

Figure 2(a) shows the conventional topology of a single-ended resistive/active feedback LNA followed by a single-to-differential (S-to-D) converter. This is the traditional solution for achieving the balun functionality in the resistive/active feedback LNA. As an alternative, a wideband balun-LNA which merges



(a)



(b)

Fig. 2. (a) Conventional topology of the single-ended LNA with negative feedback followed by a S-to-D converter, (b) proposed topology of the wideband balun-LNA merging balun and negative feedback functionality.

balun and negative feedback functionality is proposed, as shown in Fig. 2(b). This consists of a low noise S-to-D converter, a differential-to-single (D-to-S) voltage summer, a feedback network, and an output buffer. The voltage summer is used to combine the differential output of the S-to-D converter. The negative feedback exploiting wideband balun-LNA can be implemented by feeding the single-ended output signal of the voltage summer to the input of the LNA through a feedback network. The proposed balun-LNA can achieve wideband 50 Ω input impedance through a feedback resistor with balun functionality, and various types of S-to-D converters can be adopted to implement various new wideband balun-LNAs [1].

Figure 3 shows the schematic of the proposed wideband balun-LNA. In order to minimize the gain and phase imbalance, the gain of the inverting path should be equal to that of the non-inverting path. For this, the transconductance of the transistors and the load resistance are set to satisfy the following

condition:

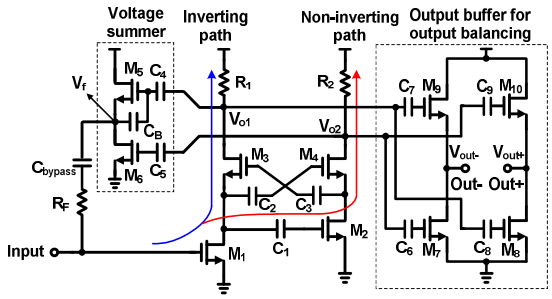


Fig. 3. Simplified schematic of the proposed wideband balun-LNA (LNA I).

$$g_{m1}R_1 = g_{m1}\frac{g_{m2}}{g_{m4}}R_2 \tag{1}$$

At low frequencies, the loop gain (T_{loop}) and the input impedance (Z_{in}) of the proposed LNA can be expressed as

$$T_{loop} \approx 2g_{m1}R_1 \tag{2}$$

and

$$Z_{in} \approx \frac{R_F + 1/g_{m5}}{1+T_{loop}} = \frac{R_F + 1/g_{m5}}{1+2g_{m1}R_1} \tag{3}$$

When the input impedance of the proposed LNA is well matched to the source impedance (R_S), the voltage gain of the proposed balun-LNA can be approximately calculated as

$$|A_v| = \left|\frac{V_{out}}{V_{in}}\right| \approx \frac{R_F}{R_S}\frac{T_{loop}}{1+T_{loop}} \tag{4}$$

The loop gain of the proposed balun-LNA is approximately two times larger than that of the conventional single-ended active feedback LNA in Fig. 2(a) using a source follower (SF). Therefore, from (3), the proposed LNA can adopt the larger value of the feedback resistor RF compared to the conventional single-ended active feedback LNA of Fig. 2(a) while maintaining the same input impedance matching. This leads to a higher voltage gain for the proposed LNA.

The dominant noise contribution in the proposed balun-LNA results from the transistor M1 and the feedback resistor RF. Assuming that all the noise sources are not correlated, the noise factor of the proposed LNA can be expressed as

$$F_{total} \approx 1 + EF_{M1} + EF_{RF} \approx 1 + \frac{\gamma}{\alpha}\frac{1}{g_{m1}R_S} + \frac{R_S}{R_F} \tag{5}$$

where excess noise factors EF_{M1} and EF_{RF} represent the noise contribution of the transistor M_1 and feedback resistor RF, respectively. Expressions for EF_{M1}

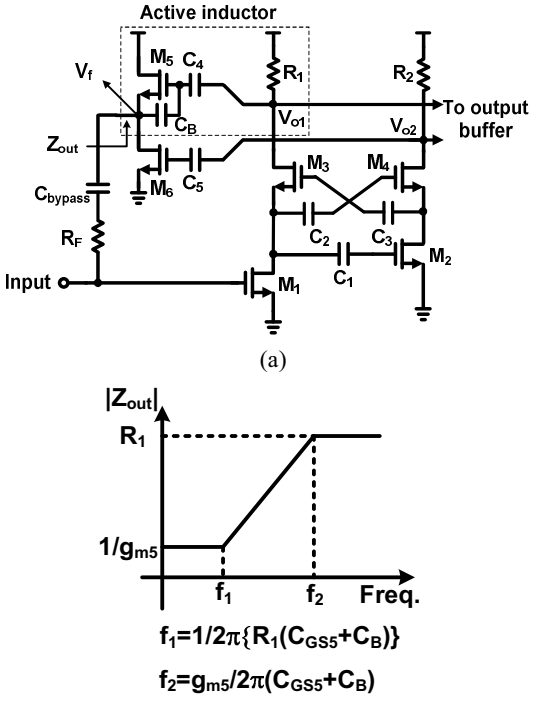


Fig. 4. (a) Common drain (CD) based active inductor in the voltage summer, (b) output impedance of the CD versus frequency.

and EF_{RF} of the proposed balun-LNA are the same as those of the conventional single-ended active feedback LNA of Fig. 2(a) derived in [2]. Therefore, from (5) it can be known that the large feedback resistor R_F resulting from the large loop gain also reduces the noise contribution from the feedback resistor compared to the conventional single-ended active feedback LNA of Fig. 2(a).

The relation between IIP3 of the open loop amplifier and IIP3 of the closed loop amplifier is given

by [3]

$$\mathrm{IIP3}_{\mathrm{closed}} \approx \mathrm{IIP3}_{\mathrm{open}}(1+T^{*}_{loop})^{3/2} \quad (6)$$

where $\mathrm{IIP3}_{\mathrm{closed}}$ and $\mathrm{IIP3}_{\mathrm{open}}$ denote the IIP3 of the closed and open loop amplifier, respectively, and T^{*}_{loop} is the loop gain of the LNA with loaded source impedance (R_S). Negative feedback can suppress the distortion components generated by the S-to-D converter within the feedback loop by a factor of the loop gain. Therefore, the enhanced loop gain of the proposed LNA improves the IIP3 as well as the gain and NF of the LNA.

The loop gain roll-off degrades the performance of the power gain, NF, and linearity at higher frequencies. The bandwidth of the loop gain is mainly dominated by the *R-C* time constant at the drain nodes of the

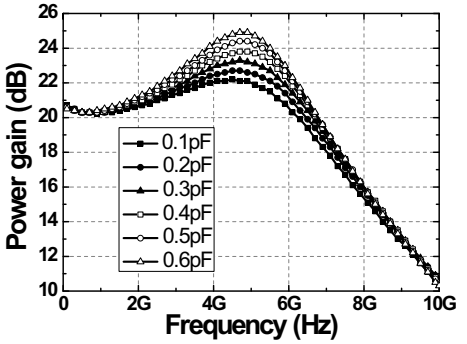


Fig. 5. Simulated power gain of the proposed balun-LNA versus bootstrap capacitance CB.

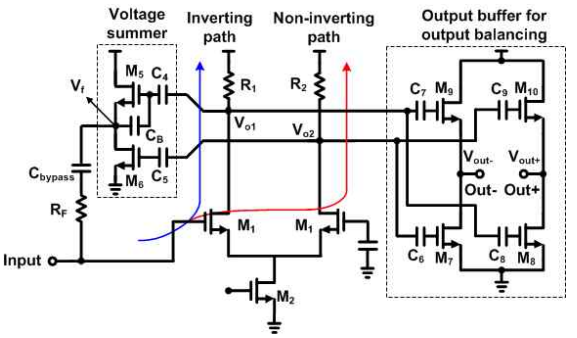


Fig. 6. Simplified schematic of the proposed wideband balun-LNA (LNA Ⅱ).

cascode transistors M_3 and M4 in Fig. 4(a). As shown in Fig. 4(a), the loop gain roll-off due to the *R-C* time constant can be compensated by using shunt-peaking of the common drain (CD) based active inductor, which consists of the transistor M_5, load resistance R_1, and bootstrap capacitance C_B. The impedance seen at the output of the CD is represented as

$$Z_{out} \approx \frac{R_1(C_{gs5}+C_B)s+1}{g_{m5}+(C_{gs5}+C_B)s} \quad (7)$$

Figure 4(b) represents the output impedance of the CD as a function of frequency. Because the output impedance of the CD is inductive between frequency f_1 and f_2, the amplification from V_{o2} to V_f in the proposed voltage summer is similar to the frequency response of a common source (CS) amplifier with peaking inductive load. This leads to a wide gain bandwidth for the proposed LNA. The bootstrap capacitance C_B provides more design freedom in controlling the inductance and the quality factor of the active inductor. Figure 5 presents the simulated power

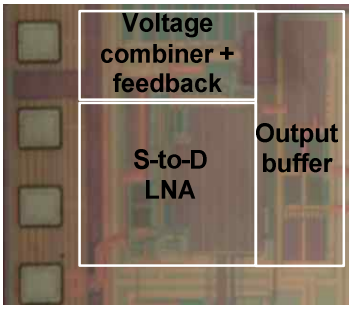


Fig. 7. Chip photograph of the proposed blaun-LNA.

gain of the proposed balun-LNA versus the bootstrap capacitance CB. The value of CB is chosen to be 0.1 pF to guarantee the stability of the non-inverting path in the proposed active feedback LNA.

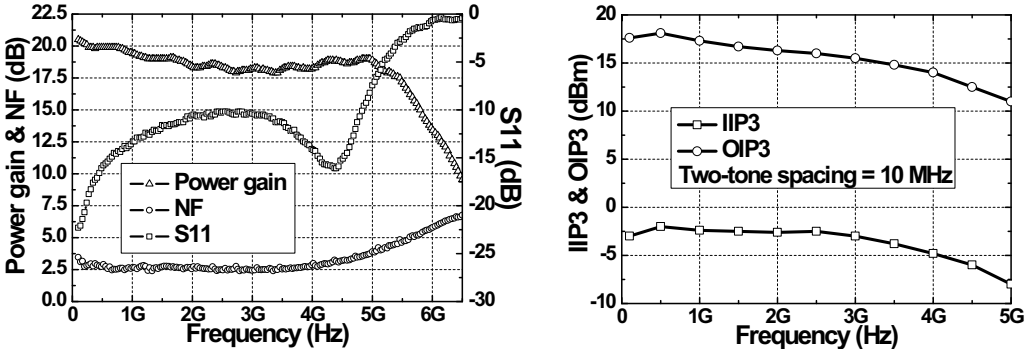
Ⅲ. Proposed Balun-LNA (LNA Ⅱ)

Figure 6 shows the proposed balun-LNA adopting the differential amplifier (M_1) with the ac-grounded second input terminal as the S-to-D converter. Compared to the LNA I, the CGCS balun load is replaced with

the differential amplifier with the ac-grounded second input terminal. If the output impedance of a current source in the differential amplifier is high enough over the entire operating frequencies and the gate of the second input terminal is ac-grounded enough over the full bandwidth, the IIP2 of the differential amplifier with the ac-grounded second input terminal is expected to be compatible to that of the differential amplifier with differential inputs. In addition, its IIP2 performance is robust to PVT variations. In simulation, IIP2 of the LNA II is at least 9 dB higher than that of the LNA I with same power consumption.

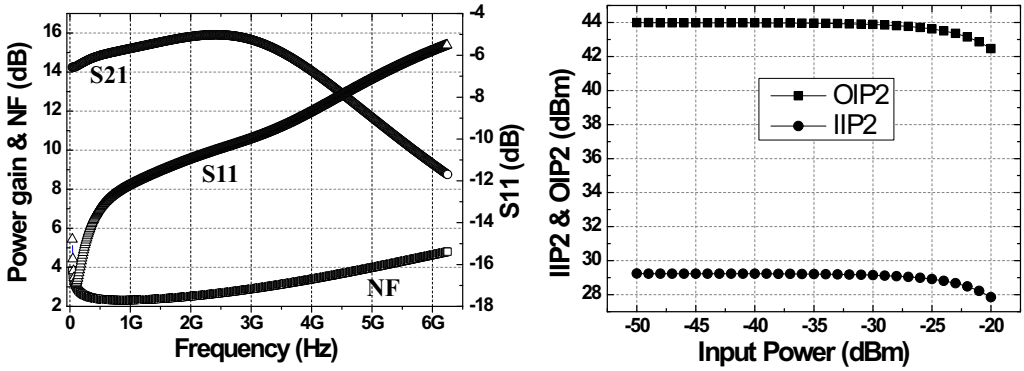
IV. Experimental Results

The proposed balun-LNA (LNA I) was fabricated in a 0.13 μm CMOS technology. Figure 7 shows the chip photograph of the proposed S-to-D LNA with an area of 400 μm × 390 μm. Wideband directional couplers were used to convert the differential signals to single-ended signals. The measurement result was obtained after de-embedding the losses by the measurement set-up. The measured power gain, S11, and NF of the proposed balun-LNA (LNA I) are shown in Fig. 8. (a) The S11 is lower than -10 dB, ranging from 100 MHz up to approximately 5 GHz, and the 3 dB gain bandwidth is above 5 GHz. The NF is below 4 dB, from 100 MHz to 5 GHz. Figure 8(b) presents the measured IIP3 and OIP3 of the LNA I over the operating frequency band. An IIP3 of -8 ~ -2 dBm is obtained over the operating frequency band. The measured IIP3 and OIP3 are slightly degraded at high frequencies because the $IIP3_{open}$ of the LNA in Eq. (6) is degraded at high frequencies. Table I summarizes and compares the performance of the proposed balun-LNA (LNA I) against those of other published data. The proposed S-to-D LNA shows higher OIP3



(a) (b)

Fig. 8. (a) Measured power gain (S21), S11, and NF, (b) measured IIP3 and OIP3 of the proposed LNA I.



(a) (b)

Fig. 9. (a) Simulated power gain (S21), S11, and NF, (b) simulated IIP2 and OIP2 of the proposed LNA II.

and comparable NF with lower power consumption compared to LNAs using 90 nm or 65 nm CMOS technologies.

The performance of the LNA II is verified through only simulation results. Figure 9(a) shows the simulated power gain, S11, and NF of the proposed balun-LNA (LNA II). It shows very wide gain-bandwidth without passive inductors, along with the proposed LNA I. Figure 9(b) shows the simulated IIP2 and OIP2 of the LNA II at around 600 MHz frequencies over the input power. It shows an OIP2 of +44 dBm and IIP2 of +29 dBm, respectively. IIP2 of the LNA II is at least 5dB higher than that of the LNA I with same power consumption.

V. Conclusions

An active feedback wideband balun-LNA employing bandwidth extension technique is proposed for SDR applications. Because the proposed balun-LNA maintains higher loop gain by summing the differential signal and feeding it to the input of the LNA, it achieves higher gain, lower NF, and higher linearity compared with conventional single-ended feedback LNA. By adopting the CD based inductive shunt peaking technique, the proposed balun-LNA can achieve a wider gain bandwidth.

TABLE I
Performance summary and comparison

	[2]	[4]	[5]	[6]	[7]	This work (LNA I)
Bandwidth (GHz)	0.2 – 3.2	1 – 10.5	0.05 – 10	0.1 – 5.2	0.5 – 5.6	0.1 – 5
Gain (dB)	11 – 15.5	16.5	18 – 20	13 – 15.6	30	18
NF (dB)	1.76 – 4.7	3.9 - 5	2.9 – 5.9	〈4	4	〈4
IIP3 (dBm)	- 9	-5	-11 – -7	〉0	-24	-8 – -2
Power consumption (mW)	25 @1.2V	36 @1.2V	22	14 @1.2 V	21.5 @ 1.2V	20 @ 1.2 V
Technology	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS	130nm CMOS

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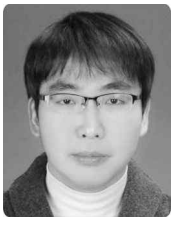

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From 2006 to 2009, he was an Associate Research Engineer with LG Electronics, Seoul, Korea, where he was involved in the development of universal analog and digital TV receiver ICs. From 2012 to 2013, he was a Post-Doctoral Researcher with KAIST, where he was involved in the development of the first RF SOI CMOS technology in Korea with SOI business team in National NanoFab Center (NNFC), Daejeon, Korea, and was responsible for the design of antenna switch, digitally tunable capacitor, power MOSFETs, and ESD devices. In 2013, he joined the Texas Analog Center of Excellence (TxACE), Department of Electrical Engineering, University of Texas at Dallas, as a Research Associate, where he developed ultra-low-power CMOS radios with adaptive impedance tuning circuits. In 2014, he joined the Division of Electronics Engineering, Chonbuk National University, Jeollabuk-do, Korea, and is now an Assistant Professor. His research interests are CMOS analog/RF/mm-wave ICs and system design for wireless communications.